

AMENDMENTS TO THE CLAIMS:

If entered, this listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (currently amended): A circuit for storing electrical energy, and consuming or supplying this energy with intrinsic protection features, comprising:

a means for the storage of electrical energy;

a means for, on the one hand, the consumption of electrical energy or

5 a means for, on the other hand, the supply of electrical energy; and

a means manufactured as integrated circuit for the secure connection of said energy storage means with said energy consumption or supply means,

whereby a switchable and controllable flow of energy between said energy storage means and said energy consumption or supply means is made possible in

10 conjunction with protection against damaging or destructive operational conditions

during said connection with said energy flowing, and where the flow of energy all

this implemented is controlled by means of integrated controllable switches

contained within an integrated switching circuit block - establishing said secure

connection – and said integrated switching circuit block which in turn itself is being

15 controlled by an integrated controller circuit block sensing and monitoring both said stored electrical energy and said consumed or supplied electrical energy and generating and delivering control signals for said integrated switching circuit block.

2. (currently amended): The circuit according to claim 1 wherein said integrated controllable switches are implemented using Field Effect Transistors (FETs).

3. (currently amended): The circuit according to claim 2 wherein said integrated controllable switches are implemented using FETs of the NMOS type with separate bulk connections.

4. (currently amended): The circuit according to claim 2 wherein said integrated controllable switches are implemented using FETs of the PMOS type with separate bulk connections.

5. (currently amended): The circuit according to claim 1 wherein said means of integrated controllable switches within an integrated switching circuit block is realized with two FETs, serially connected in a cascade circuit between said energy storage means and said energy consumption or supply means, thus forming a mid node between said two serially connected FETs.

6. (currently amended): The circuit according to claim 5 wherein said mid node is connected via an additional integrated controllable switch to the integrated controller circuit block monitoring both said stored electrical energy and said consumed or supplied electrical energy.

7. (currently amended): The circuit according to claim 6 wherein said additional controllable integrated switch is implemented as FET.

8. (currently amended): The circuit according to claim 6 wherein said additional integrated controllable switch is closed and wherein one of said two FETs, which are serially connected in a cascade circuit, is operated as a source follower.

9. (original): The circuit according to claim 1 wherein said means for the storage of electrical energy is a battery.

10. (currently amended): The circuit according to claim 1 wherein said means manufactured as integrated circuit (IC) for the secure connection of said energy storage means with said energy consumption or supply means is implemented as a monolithic integrated circuit (IC) device.

11.(original): The circuit according to claim 10 wherein said IC device is realized in CMOS technology.

12.(original): The circuit according to claim 10 wherein said IC device is realized in CMOS deep well technology.

13.(original): A circuit for battery charging and discharging with intrinsic protection features, comprising:

5 a battery with two terminals, called the one and the other battery terminals, each being either of the positive or the negative terminal type;

a load or charger two-pole device with two terminals each;

a first FET switch having gate, source, drain, and a separate bulk, wherein said drain is coupled to one battery terminal;

10 a second FET switch having gate, source, drain, and a separate bulk, wherein said drain is coupled to said first FET switch source to thereby form a mid node and wherein said source is coupled to a load or charger terminal; and

15 a means for controlling said first and second FET gates together with said separate bulks wherein the gate voltages of said first and second FET switches determine the OFF and ON states of said first and second FET switches, and wherein said first FET separate bulk is switchable coupled between said one battery terminal and said mid node, and wherein said second FET separate bulk is switchable coupled between said mid node and said load or charger terminal and

wherein another additional controllable switch is connected between said other battery terminal and said mid node.

14. (original): The circuit according to claim 13 wherein said first and said second FET switches comprise NMOS FET devices connected between said one battery terminal - which is of the negative battery terminal type – and the load or charger terminal, whereas the other battery terminal is of the positive terminal type.

15. (original): The circuit according to claim 13 wherein said first and said second FET switches comprise PMOS FET devices connected between said one battery terminal - which is of the positive battery terminal type - and the load or charger terminal, whereas the other battery terminal is of the negative terminal type.

16. (original): The circuit according to claim 13 wherein said means of controlling said first and said second FET gates together with said separate bulks further comprises charge pump circuits for securely generating the ON state voltages for said cascaded FET switches and for said separate switchable bulk coupling devices.

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17. (original): The circuit according to claim 13 wherein said FET switches and said means of controlling comprise a single monolithic integrated circuit (IC) device.

18.(original):The circuit according to claim 17 wherein said IC device is manufactured in CMOS technology.

19.(original):The circuit according to claim 17 wherein said IC device is manufactured in CMOS deep well technology.

20.(original):The circuit according to claim 13 wherein said first FET switch separate bulk is coupled to said mid node and said second FET switch separate bulk is coupled to said load or charger terminal and wherein said other additional controllable switch connected between said other battery terminal and said mid node is open during battery charging.

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21.(original):The circuit according to claim 20 wherein said first FET switch and said second FET switch are turned to said ON state during normal charging.

22.(original):The circuit according to claim 20 wherein said first FET switch and said second FET switch are turned to said OFF state during over charging.

23.(original):The circuit according to claim 20 wherein said first FET switch acts as a MOS diode and said second FET switch is turned to said ON state during charging in a battery over discharged state.

24.(original):The circuit according to claim 13 wherein said first FET switch separate bulk is coupled to said one battery terminal and said second FET switch separate bulk is coupled to said mid node during battery discharging.

25.(original):The circuit according to claim 24 wherein said first FET switch and said second FET switch are turned to said ON state during normal discharging.

26.(original):The circuit according to claim 24 wherein said first FET switch is turned to said OFF state and said second FET switch is turned to said ON state during over discharging.

27.(original):The circuit according to claim 24 wherein said first FET switch is turned to said ON state and said second FET switch acts as a MOS diode during discharging in a battery over charged state.

28.(original):The circuit according to claim 24 wherein said first FET switch is turned to said OFF state and said second FET switch is turned to said ON state, acting as a source follower and wherein said other additional controllable switch connected between said other battery terminal and said mid node is closed during strongly discharging in an inverted voltage charger state (i.e. operating in reverse condition).

29.(original):The circuit according to claim 13 further comprising:

 a voltage divider having an output setting up a voltage value between said one battery terminal voltage and said load or charger terminal voltage; and
 a means of coupling said voltage divider output and said mid node.

30.(original):The circuit according to claim 29 wherein said means of coupling comprises a FET switch device.

31.(original):The circuit according to claim 30 wherein said FET switch device is turned to the ON state in the case of over charging, i.e. when the first FET switch and the second FET switch are both turned OFF during over charging.

32.(original):The circuit according to claim 29 wherein said voltage divider is connected via an additional diode device to said one battery terminal.

33.(original):The circuit according to claim 29 wherein said FET switches and said means of controlling comprise a single monolithic integrated circuit (IC) device.

34.(original):The circuit according to claim 33 wherein said IC device is manufactured in CMOS technology.

35. (original): The circuit according to claim 33 wherein said IC device is manufactured in CMOS deep well technology.